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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,254	02/12/2004	Yasuyuki Hori	1460.1045	4159

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EXAMINER	
SCHLIE, PAUL W	
ART UNIT	PAPER NUMBER
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,254	HORI, YASUYUKI	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, and 7-9 have been examined as amended 1/05/07, with claims 5-6 being canceled.

Response to Arguments

2. Applicant's arguments filed 1/05/07 with respect to the rejection of claims 4 and 6 have been fully considered and are persuasive, and thereby withdrawn.

3. Applicant's remaining arguments have been fully considered but not persuasive and/or moot in view of their continued rejection as necessitated by amendment.

As Thankrakul is considered to broadly teach the means claimed by which a reprogrammable program memory may be reprogrammed by temporarily utilizing program and transfer buffer memories; which in combination with that considered well known to one of ordinary skill in the art, being that any combination of suitable memory technologies, either internal or external, may correspondingly be utilized for their intended purpose; and that such memories must be correspondingly enabled as a necessary function of the state of the reprogramming process to achieve that taught; all claims are considered correspondingly obvious to one of ordinary skill in the art.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1-4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thantrakul (5,784,611).

As per independent claim 1, Thantrakul teaches a microcontroller system and/or method comprising: an embedded processor; a potential plurality of addressable internal and/or external volatile and non-volatile memories within which may themselves contain non-volatile reprogramming code (see figures 6-11); and reprogramming logic comprising mode select signals (see ISPA*, ISP Switch and CSDS in figure 7) where upon detection of said mode select after reset, said logic may be configured to logically remap said memories (and/or inherently regions of said memories) to enable the execution of said reprogramming code and logical access to target reprogrammable memory as may be required to enable it's sequential reprogramming from some data source by said embedded processor (see figure 8). Correspondingly the logic in (figure 7) clearly depicts a circuit enabling a reprogrammable non-volatile memory; accessible as a source program memory when operating in a normal mode enabled by a first chip select, or alternatively accessible as a destination data memory when operating in a re-program/re-write mode enabled by a second chip select in lieu of a volatile memory otherwise being accessible by said second chip select when operating in a normal mode (see figure 7, "RDMCS* signal, To Microprocessor Flash/EEPROM Memory"); which in combination with that considered well known to one of ordinary skill in the art, being that any combination of suitable memory technologies, either internal or external,

may correspondingly be utilized for their intended purpose; and that such memories must be correspondingly enabled utilizing logic (selector circuit) as a necessary function of the state of the reprogramming process to achieve that taught; all claims are considered correspondingly obvious to one of ordinary skill in the art.

As per claims 2-4 and 7-9, being dependant on claim 1, or correspondingly dependent claim inclusively, Thantrakul further teaches that said reprogramming code may be transferred from its initial storage/source location to volatile memory prior to executing said reprogramming code from said volatile memory (see figure 9A), and enables the selection of an initial logical address mapping of said memories upon power-on/reset (see figure 8).

Where although the terminology utilized by the reference may differ from that claimed, all limitations within claims 1-4 and 7-9 are considered clearly taught, or correspondingly obvious in combination with that well known to those of ordinarily skill in the art at the time of the claimed invention.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765, or email address [paul.schlie@uspto.gov]. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
2/1/07